REMARKS

Claims 1-12 remain in the application. Claims 1-12 stand rejected.

The Examiner objected to the disclosure in that it contained a grammatical error in the summary of the invention, first paragraph, line 3. The Examiner is correct and this error has been corrected.

The Examiner rejected claims 3, 4, 5, 8 and 9 under 35 U.S.C. § 112, second paragraph as being indefinite.

Applicants have considered the text of the Examiners rejection in some detail and can find no objection to claim 3.

In paragraph 5 of the office action, the Examiner objected to the limitation of claim 4 at lines 58 and 59. The language which the Examiner found objectionable has been corrected.

In paragraph 6 of the office action, the Examiner objected to claim 4 in that it contained a phrase "such as." Claim 4 has been amended to change the language.

In paragraph 7 of the office action, the Examiner objected claims 8 and 9 as lacking appropriate antecedent basis for the limitation "the processing element" in line 2. That phrase also exists in each of claims 6-9. The antecedent for "the processing element" is found in claim 5 from which all of those claims depend.

In paragraph 8, the Examiner objected to the use of the term "etc." in claim 4, line 54. The Examiner is correct and the language has been changed to more adequately describe the invention.

In paragraph 11 of the office action, the Examiner rejected claims 1-7 under 35 U.S.C. 103 as unpatentable over "applicants own admission (i.e., specification (AOA)) in view of Pillage et al." The Examiner states:

> "AOA and Pillage are analogous since they both teach logic circuits.
>
> Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the vector space of Pillage in the logic circuit of AOA because Pillage teaches a method to provide an improved method and apparatus for simulating behavior of a microelectronic interconnect circuit at higher speeds than conventional circuit simulators."

The Examiner's rejection is somewhat confusing because Pillage does not have a vector space. Further, Pillage mentions the word "logic" in only two places. The first, is in the title of a patent to a third party referenced in column 1, lines 41-44. The second reference occurs in column 6, lines 5-7 referring to the contents of circuit libraries used in prior art design systems.

The Pillage reference has nothing to do with simplifying logic. The problem to which Pillage is directed to is addressed as follows:

> "As the feature sizes of integrated circuits, the characterization of the parasitic effects associated with the interconnect path among the active devices becomes more critical and more difficult. In the past, the effect of interconnects could simply be disregarded when simulating the operation of an integrated circuit, because the active circuit elements dominated the simulation in terms of delay. However, as the feature sizes of

> integrated circuits continue to shrink, the metal resistance per unit length tends to increase and the switching speeds tend to increase. In addition, the close proximity of metal lines makes the component cross-talk capacitance larger. Even inductance effects, which are evident for boards and multichip modules which comprise microelectronic systems, may also be important for modeling the integrated circuit packaging or chip-to-package interface. Accordingly, a complete circuit simulation of an integrated circuit must now account for the resistive, inductive and capacitive effects of the interconnect paths in addition to simulating the effect of the active devices on the integrated circuit."

In conventional circuit simulators such as a Spice simulator, it may be possible to do a complete characterization of an integrated circuit. However, the complete simulation becomes extremely time consuming and may exceed the storage capacity of the processing system in which the simulation is run. See column 2, lines 13-22.

Pillage describes the Asymptotic Wave-form Evaluation (AWE) System which provides "a generalized approach to linear resistor-inductor-capacitor (RLC) circuit response approximations. See column 2, lines 23-32. Pillage states:

> "AWE is a general method for computing any number of moments for any linear circuit. Using the method, a qth order approximation to the actual circuit response can be obtained by computing 2 q moments of the circuit and matching these moments to the circuit's impulse response. The moments, in their simplest interpretation, represent the coefficients of the s-terms in the Taylor series expansion of the homogenous circuit response. Once the desired number of moments are found, they may be mapped to the dominant poles and corresponding residues. Once the poles and residues of the approximate response are found, the time domain response of the interconnect circuit may be determined.
>
> In the AWE technique, moments of a circuit may be generated by successively solving an equivalent DC circuit with all

> capacitors replaced by current sources and all inductors replaced by voltage sources." See column 2 line 32-49.

The AWE system has limitations. Sometimes "moment matching techniques may yield unstable models having positive time constants (positive poles) for linear, passive (stable) circuits. This instability can be mainly attributed to two phenomena: (1) the extreme sensitivity of the moment values to numerical noise, and (2) the zero locations that characterize the high frequencies associated with impulse- and step-response approximations."

The Pillage invention, as summarized beginning column 3, is to provide ways to overcome the limitations of the AWE method discussed above.

The way in which Pillage achieves this is described in conjunction with Figure 3. Step 20 of Figure 3 shows storing a representation of an interconnect circuit. Such an example is shown in Figure 18A. That representation is then transformed into an equivalent DC circuit, such as shown in Figure 18B.

The equivalent DC circuit is converted into a directed graph as shown in Figure 18C. And then a spanning tree is constructed from the directed graph as discussed in conjunction with Figure 18C.

Thus, Pillage has nothing to do with a vector space and has nothing to do with "representing logic of a logical circuit to be designed as points and vectors in a vector space as required by the claims. Pillage does not represent logic as points and a vector in a vector space and does not utilize the points and vectors in that vector space to simplify the logic of the logical circuit represented.

The Examiner has not clearly defined what it is that the Examiner considers to be an admission of prior art. The Examiner, at page 7 of the previous office action (May 19, 2006), last line, and continuing on to page 8, identifies the admission of prior art with reference to the specification "pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 'logical device' 'simplification machine'". There is a second reference on page 9 of the office action, when addressing claim 4, to page 11, paragraph 1-2 and 6 of the specification. For clarity, applicant believes that the first reference to admissions of prior art on page 24 refers to the following text:

> More than ten years ago the National Academy of Sciences Panel on Photonics Science and Technology Assessment declared that "The ultimate benefit of Photonic processing could occur if practical optical logic could be developed" (Whinnery et al., *Photonics*, 1988, p. 35). So far the implied challenge of the Panel has not been met.
>
> Vector manipulation has been one of the big success stories for optical computation, but vector techniques themselves promise an application to the logic of optical computation as a whole. The full ANS-/CNS- space could be built as an optical device for checking the validity of arguments or as a logic device for optical computation, and also as simplification machine. Each operation in the space is a laser, and the resultant proposition-points such as **p** and **pq** and **pqr** are multifaceted beamsplitters or mirrors which reflect the beams in the correct logical directions at the correct logical strengths to ensure the required implications.

First, applicant traverses the Examiner's determination that these paragraphs constitute an admission of prior art. The Examiner has not made clear what it is from these paragraphs that should be taken or combined with the Pillage reference even if these paragraphs could be considered an admission of prior art. Second, the Examiner has failed to provide any rationale for the combination of any portion of the text of the specification with the Pillage reference. Thus, the Examiner has failed to establish a prima facie case of obviousness, and has failed to

establish a prima facie case that applicant has admitted anything in the paragraphs set forth on page 24. Page 24, in context, is a description of the invention that applicants have invented.

The first paragraph quoted from page 24 clearly acknowledges that practical optical logic has not been developed, at least until this application. The second paragraph distinguishes "vector manipulation" from "vector techniques." Some optical devices do process vectors but the vector techniques in accordance with the invention promise an application of the logic of optical computation as a whole. The statement about the "full ANS-/CNS- space could be built as an optical device for checking the validity of arguments or as a logic device for optical computation, and also as a simplification machine" refers to applications of the inventors techniques described in this application and not to prior art.

Turning to page 11 of the specification, the Examiner refers to paragraphs 1, 2 and 6.

The first paragraph on page 11 acknowledges that a practical method for reducing truth-functional schemata continues to be "surprisingly elusive." Paragraph 3 on page 11 talks about applicants own invention and how that problem can be solved. Similarly, paragraph 6 on page 11 discusses applicant's invention and it does not constitute an admission of prior art.

The supplemental information provided by the Examiner on pages 4 and 5 of the office action of December 12, 2006 similarly do not address how one would combine what the Examiner considers an admission of prior art with the Pillage reference even if it were an admission, which it is not. Thus the Examiner has failed to establish a prima facie case of obviousness.

Thus, each of the portions of the specification to which the Examiner points as constituting admissions of prior art do not, in fact, constitute admissions of prior art.

Further, the Pillage reference does not represent logic of a logical circuit as points and vectors in a vector space as required by independent claims 1, 2, 3, 5, 10, 11 and 12. Thus, each independent claim and all of their dependent claims contain claim language that is not met by Pillage. The portions of the specification relied on by the Examiner as constituting "admissions of prior art" do not provide any teaching or suggestion which would overcome the deficiencies in the Pillage reference, even if they were admissions of prior art, which they are not.

Accordingly, the Examiner is requested to reconsider the rejection of claims 1-7 under 35 U.S.C. § 103 as based on Pillage in view of an admission of prior art.

The Examiner rejected claim 8 under 35 U.S.C. § 103 as unpatentable over Pillage in view of the purported admission of prior art and Chan.

Claim 8 is dependent upon claim 5 and recites that the "processing element is an colorimetric computer."

Chan does not disclose a colorimetric computer. Rather, Chan is directed to translating values from an adjustment color space controlled by a user to a printer color space and doing so in a way that the adjustments appear to be perceptually uniform.

The purpose of the Chen patent is to overcome problems of the prior art described in column 1, lines 12-26. There it states:

> "Systems exist that allow a user to create, modify, and print color images. [See Figure 5] These printing systems typically consist of a general purpose computer, a monitor or other viewing device, and a printer.
>
> Some printing systems allow a user to make contrast and other color adjustments to a printed image. However, these adjustments are typically performed in the monitor's color space or in the printer's color space. Therefore, the resulting changes in the printed image are perceived as highly non-linear and unpredictable when compared to the user-input adjustments. This is because the color spaces that are used to make the adjustments are not visually uniform. That is, the adjustments defined by the user are not carried out by the system in a perceptually uniform manner, as perceived by the human eye." [Bracketed information added]

The Examiner has made no showing why it would have been obvious to adapt information from a patent on a computer printing system and to apply that to the claimed invention. The Examiner has not provided a rationale why it would be obvious to apply any portion of the Chan patent to Pillage or to the alleged admission of prior art by the applicants in such a way as to meet claim 8. Accordingly, the Examiner has failed to establish a prima facie case of obviousness.

The Examiner rejected claim 9 under 35 U.S.C. § 103 as unpatentable over Pillage in view of applicants alleged admission of prior art and further in view of Yount.

Yount is directed to an automatic flight control system that is fail safe in that there are at least two independent subsystems, one of which includes a dual channel flight control computer. Data is processed redundantly and if disagreement occurs between one of the two processing elements in a channel or between two processing elements and a different processing element, an error is declared and the data is not relied on. The Examiner states:

> "It would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize Yount and

> Pillage in AOA because Yount teaches data processing to reduce safety hazards resulting from generic faults in the software or the processors (Yount: column 1, lines 10-12)."

The Examiner has failed to link the redundant data processing techniques of Yount to the system of Pillage in any way that would teach or suggest the application of Yount to Pillage or to the alleged AOA.

Accordingly, the Examiner has requested to withdraw the rejection of claim 9 based on the references applied.

The Examiner rejected claims 10-12 under 35 U.S.C. § 103 as unpatentable over Pillage in view of applicants alleged admission of prior art and further in view of Eng.

The Eng reference is directed to improving the speed of a top down design process. Figure 1 shows the prior art top down design flow process and the right hand side of Figure 1 shows the improved RTL (Register-Transfer-Level) optimization design flow of the claimed invention. The problem to which the Eng patent is direct is the "design gap" between what semi-conductor vendors can manufacture with modern deep sub-micron processes and what designers can create using top down electronic design automation design tools. The conventional top down design tools were originally designed in an era when gate delays dominated chip timing. The top down EDA tools use inaccurate statistical wire-load estimates to model wiring parasitics at early stages in the design cycle and the effect of those inaccuracies are propagated throughout the rest of the design methodology. To overcome that problem, the Eng invention utilizes the optimized design flow shown in the right hand side of Figure 1.

It is not clear at all how the Examiner proposes to combine Eng with Pillage let alone with the alleged admission of prior art to meet the terms of the claim language. Further, as noted above, none of the references applied by the Examiner represent logic of a logical circuit as points in vectors in a vector space as required by each of the claims. Accordingly, applicant respectfully requests that the Examiner withdraw the rejection of claims 10-12 under 35 U.S.C. in view of Pillage, the alleged admission of prior art and Eng.

On pages 4-7 of the office action, the Examiner attempts to address what the admission of prior art constitutes and what the reference is to Pillage, Chan, Yount and Eng supposedly teach. Nevertheless, the Examiner has made no attempt whatever to map the contents of the references nor of the supposed admission of prior art to the language of the claims.

Accordingly, the Examiner has totally failed to establish a prima facie case of obviousness of the claimed invention.

Accordingly, applicants respectfully request that the Examiner reconsider the rejections, withdraw them and allow the claims to issue as a patent.

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Respectfully submitted,

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